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Fraunhofer IZM Institut Zuverlässigkeit und Mikrointegration

Imprint

2. International Symposium on Photonic Packaging

Fraunhofer IZM Institut Zuverlässigkeit und Mikrointegration

Electrical Optical Circuit Board and Optical Backplane

organized by Fraunhofer IZM, co-organized by VDI/VDE-IT, IEEE-CMPT, IEEE-LEOS

November 13, 2008, Electronica, Messe München | Hall A1 Conference Room A12, 9:30 am – 5:30 pm

Program

» System Design

09:30-09:40	Welcome *Henning Schröder* Fraunhofer IZM Berlin, Germany
09:40-10:10	Optical Interconnect Applications for Multimode Siloxane Components *Ian H. White* University of Cambridge, Cambridge, UK
10:10-10:40	Design Rules for Polymer Waveguides and Measurement Mechniques *Kai Wang* University College London, London, UK
10:40-11:10	CAD of Board-Level Optical Interconnects *Jürgen Schrage* Siemens C-Lab, Paderborn, Germany
10:40-11:10	Coupling Light to and from Optical Boards *Peter van Daele* University of Gent, Gent, Belgium
11:40-12:30	Lunch break

» Components

12:30-01:00	240 Gbit/s Parallel Optical Transmission Using Double Layer Waveguides in Thin Glass Sheets *Henning Schröder* Fraunhofer IZM Berlin, Germany
01:00-01:30	Flexible Optical Interconnects *Geert van Steenberge* University of Gent, Gent, Belgium
01:30-02:00	Refractive Index Profiling of Polymer Planar Optical Waveguides Using Optical Coherence Tomography *David Ives* National Physical Laboratory, Middlesex, UK
02:00-02:30	Ink Jet Printing of Optical Waveguide Material *John Chappell and David Hutt* Loughborough University, Loughborough, UK
02:30-03:20	Coffee break

» Integration Technologies

03:20-03:50	Transfer of Polymer Waveguide Fabrication Processes to a Commercial PCB Foundry *Dougal Stewart* Stevenage Circuits Limited, Stevenage, UK
03:50-04:20	Board-Level Optical Interconnects for Computing Applications *Bert Offreins* IBM Research Labs, Rüschlikon, Switzerland
04:20-04:50	Pluggable Interconnect Technology for Electro-Optical PCBs *Richard Pitwon* Xyratex, Hampshire, UK
04:50-05:20	Optoelectronic Printed Circuit Board Realised by Two Photon Absorption Structuring *Gregor Langer* AT&S AG, Leoben, Austria
05:20-05:30	Final Remarks *Henning Schröder* Fraunhofer IZM Berlin, Germany

VDI|VDE|IT · CPMT IEEE Components, Packaging and Manufacturing Technology Society German Chapter · IEEE LEOS The Society for Photonics

Flexible Optical Interconnects

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Abstract—**This paper presents the development of an optical interconnect embedded in a flexible substrate, including embedded optical waveguides, light sources, and detectors. Commercially available VCSEL and photo-detector (PD) chips are thinned down to 30 _m, embedded into a flexible foil of optical transparent material and coupled by means of embedded waveguides and out-of-plane micro-mirrors. The resulting structure shows very good flexible behavior and low optical losses.**

flexible optical interconnect, photo-detector, polymer waveguide, VCSEL.

I. INTRODUCTION

The drive for looking into such integration comes from a variety of applications. Amongst these one can identify e.g. an increasing use and interest in optical fibres for sensing applications, triggered by their many advantages (EMI immunity, high sensitivity, parallel read-out capacity…). For these applications, the fibre sensors need to be coupled to optoelectronic sources, detectors, etc. and the proposed flexible embedded optical interconnections offer a highly integrated solution.

The flexible character of the substrate opens ways to use such substrates as foils over irregular surfaces (e.g. for distributed sensing applications), on moveable surfaces (e.g. in robotics) or to be folded into compact modules (for portable devices, automotive, etc). The flexible behavior enables cheap production processes like roll to roll production which have been shown for flexible electrical interconnections.

Embedding optical interconnections counter the fundamental bottlenecks of electrical interconnections such as speed, packaging, fan-out and power dissipation. Many research institutes (including ours [1]) have proven the integration concept on a rigid printed circuit board. The technology and the demonstrator in this paper take these optical interconnections one step further to flexible substrates.

II. FLEXIBLE OPTICAL WAVEGUDIES

Within the range of materials that can be used for the optical layers, we have chosen for the use of Truemode™ Backplane Polymer [2], Ormocer® [3] and Epocore [3] materials to meet the requirements in view of their temperature stability, optical and chemical properties, manufacturability and compatibility with PCB processing. The optical materials are however not flexible and strong enough to be bended without cracking or damaging. Therefore these layers are sandwiched between two Polyimide (PI) layers, one at the top and one at the bottom, which absorb all stress and pressure during bending, see Figure 1. Polyimide has been chosen because of the existing know-how of electrical assembly on Polyimide. It is the dominant material in the flexible circuits industry because of its good electrical, chemical, temperature and mechanical behavior [4].

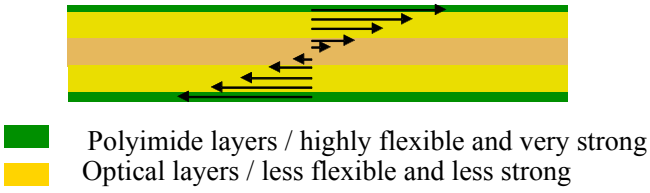

Figure 1 Symmetrical layer build-up releases the stress from the inner layers.

Patterning of the core-layer to create multimode 50 μm x μm waveguides is carried out using either a standard photolithography process or by laser ablation using a 248 nm wavelength KrF Excimer laser.

Optimization of the technology for structuring waveguides using laser ablation has been reported in earlier research for rigid substrates [1], and can be applied for flexible substrates, as all flexible layers are processed on a temporarily rigid carrier which is released at the final stage of the process-flow. The resulting stacks of optical- and PI- layers show good adhesion and very good flexible behavior (down to bending radii of a few millimeters), see Figure 2. The fabricated waveguides have low propagation losses (below 0.15 dB/cm) and low bending losses (below 0.15 dB/cm for a bending radius of 15 mm, and below 0.25 dB/cm for a bending radius of 8 mm).

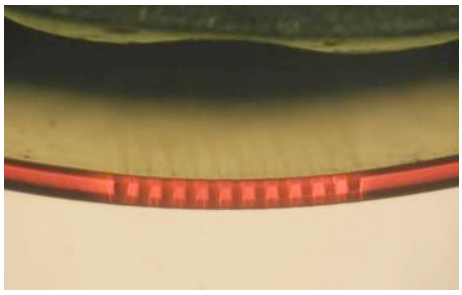

Figure 2 Completed optical foil in Truemode™ Backplane Polymer, bended with radius of curvature of 1 cm.

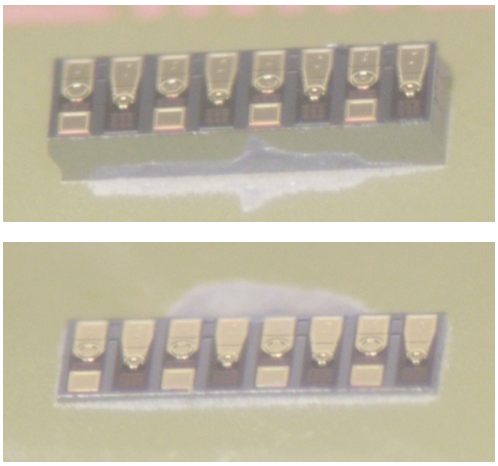

Figure 3 Microscope images of a standard 150 _m thick VCSEL array (up), and a 30 _m thinned VCSEL array (down).

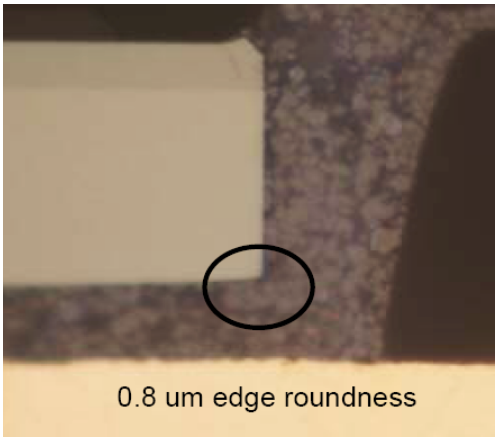

Figure 4 Cross-section of a thinned VCSEL array, showing the absence of edge damage.

III. Flexible (opto-) electronic devices

Embedding rigid components like VCSEL and PD chips inside a flexible substrate, asks for special measures to ensure the flexibility. Standard commercially available optoelectronic components have a typical thickness of 150 _m. Since we have to apply Polyimide layers and waveguide layers on top of the embedded die, the total thickness will become too large to ensure good substrate flexibility. To counter this problem, a thinning process for the dies has been developed to reach thicknesses smaller than 30 _m. This way dies have even proved to be bendable, increasing the reliability of the package.

The naked dies are mounted face down onto a temporary rigid glass carrier with a dedicated wax, together with large dummy GaAs chips. This carrier is attached to a jig which rotates on a lapping disk which also rotates. The lapping disk is covered with slurry. This slurry contains grains of Al_2O_3, which removes material from the dies on a respectively mechanically or chemical basis. The jig itself can apply a controllable force on the dies. Because of the small dimension of the VCSEL and PD arrays (1000 _m x 250 _m) the applied load on the die is too high. Dummy GaAs dies are mounted therefore around the functional dies during the lapping process to divide the load over a larger area.

Fast processing is an advantage but is inherent connected to higher surface damage. This is why we split the thinning process into two consecutive steps. First a fast lapping step with a grain size of 9 _m, achieving a lapping speed of ± 20 _m per minute. The large grain size damages the die surface, which is than resolved by a polishing step with a grain of 0.3 _m thickness (lapping speed of 0.2 _m per minute). Fine-tuning of the different process parameters resulted in a low final backside roughness of the die, no surface damage, small edge roundness of 0.8 _m and a high yield. Figure 3 shows a thinned VCSEL array, and Figure 4 the low edge roundness.

IV. Embedding opto-electronic devices

Figure 5 shows the schematic overview of the process flow to embed thinned VCSEL and PD array chips in a flexible foil, coupled by embedded waveguides and 45˚ mirror structures.

For planarization reasons, the VCSELs and PDs are mounted in a cavity inside the under cladding layer, structured using the KrF Excimer laser, enabling accurate cavity dimensions.

In Figure 5, the blue part stands for the rigid glass carrier, the green layer is the bottom PI layer and the yellow layer is the under cladding layer. In between the under cladding layer and the PI layer, a metal island is deposited. This acts as a heat sink for the active components and also as a laser stop.

The active components are mounted inside the cavity with a low temperature curable adhesive. The adhesive needs to be heat conductive but not electrical conductive and needs to show very low viscosity to fill the whole cavity.

To reach the high alignment requirements and coupling efficiencies, it is necessary that the die is perfectly leveled with the substrate surface and not tilted. After placing the die in the adhesion filled cavity, leveling can be achieved by pressing the die into the cavity as shown in Figure 5. This way the tilt of the chip is lower than 1 degree.

In the next step the die is covered with a cladding layer of 10 _m to finish the embedding of the die. This layer has proven to be well planarized. Laser defined micro-vias are drilled to the embedded contact pads and metalized. Metallization is needed to fan out the small pitch contact pads of the embedded VCSEL and PD arrays (250 _m pitch) towards larger pitch contact pads (2 mm pitch) on the substrate surface

The production of waveguides on top of the embedded dies is done using standard lithography and an alignment error in relation to the active area of the opto-electronic components is within 5 _m. Out-of-plane turning mirrors are defined using KrF Excimer laser ablation. The whole structure is then again covered with a cladding layer to cover the metalized mirror and to obtain final planarization.

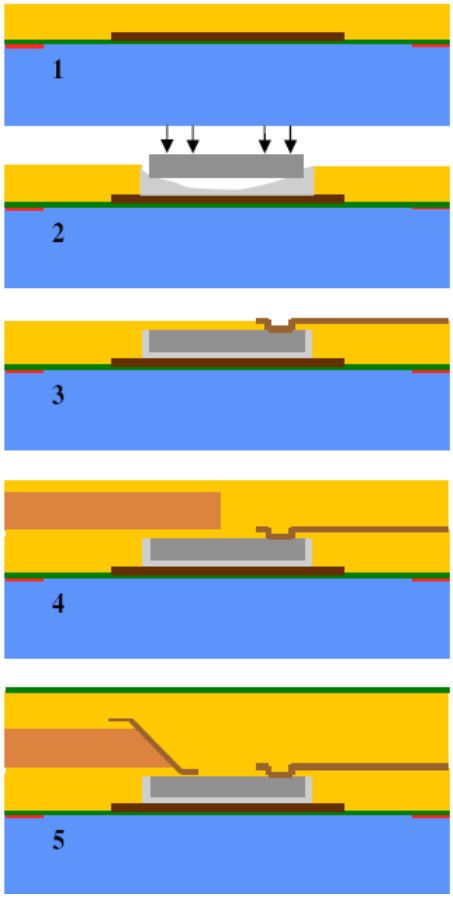

Figure 5 Schematic overview of the process flow to embed optoelectronic components in a flexible foil.

Figure 6 shows a cross-section of an embedded VCSEL array in Truemode™ Backplane Polymertogether with the micro-mirror and the galvanic interconnection.

On top of the upper cladding layer a final PI layer is spin-coated to finish the layer build-up. Laser ablation of the edges enables the release of the rigid carrier. After release the substrate shows no war-page or curling because of the symmetrical build-up. The flexibility of the optical foil is demonstrated in Figure 7.

The optical power loss for the complete embedded flexible link is currently below 10 dB. In addition to lowering this loss budget, future research is directed towards the thermal management of the embedded actives, and the coupling with optical sensors, to allow for a fully integrated optical sensing foil.

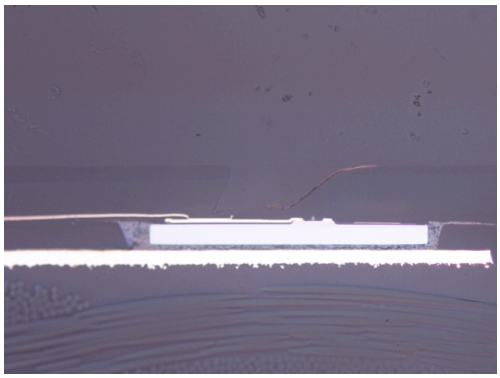

Figure 6 Cross-section of an embedded VCSEL array in Truemode™ Backplane Polymer together with the micro mirror and the galvanic interconnection.

Figure 7 Flexible optical foil with embedded waveguides, coupling structures, VCSEL and PD chips, and electrical fan-out.

ACKNOWLEDGMENT

Part of this work was carried out within the framework of the PHOSFOS project (Photonic Skins For Optical Sensing), supported by the European Commission through the 7th Framework Program, and the authors would also like to thank the Flemish IWT (Institute for the Promotion of Innovation by Science and Technology) for financial support through the FAOS project (Flexible Artificial Optical Skin).

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